REMARKS

Claims 16, 18, 21 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Lim et al. (U.S. Patent No. 6,613,652) (hereinafter: "Lim").

Applicants respectfully request reconsideration and removal of this rejection. Lim fails to support a case of anticipation of claims 16, 18, 21 and 22 of the present application under 35 U.S.C. § 102 because of differences in structure, operation and effect. These differences are explained below.

Regarding claim 16, the bonded SOI substrate according to claim 16 of the present application and the semiconductor of Lim differ structurally in the heights of cavities formed in the device. Specifically, the heights of all of the cavities (identified by numeral "16" in Fig. 6B) in Lim are the same. The heights of the cavities as recited in claim 16 in the present application and as shown in Figs. 3c and 3d are different.

In the present invention, by varying the heights of the cavities, that is, by changing the thickness of the active layer ("10A" in Fig. 3) directly on top of the cavities, the semiconductor of claim 16 of the present invention leads to a reduction in parasitic capacity arising between the silicon wafer and metal interconnections within the device when the heights of

the cavities are large (the active layer is thin) and enables bipolar elements to be formed in the regions where the cavities are small (the active layer is thick). Therefore, CMOS logic, which requires higher performance than other devices, is fabricated in thin active layers to exhibit its characteristics sufficiently. On the other hand, memory functional blocks and analog function blocks are larger devices than CMOS logic, and are fabricated in the thicker active layers.

In addition, the shape of the cavities of the bonded SOI substrate as recited in claim 16 of the present invention is circular or polygonal in a plan view.

According to claim 16 of the present invention, it is possible to fabricate a plurality of devices with different functions within a single chip because the heights of the cavities are different.

On the other hand, since one type of device is fabricated in the active layer (Figs. 6B and 10B, for example) in Lim, the heights of the cavities are all the same and there is no need for the heights to vary. In Lim, there is nothing to suggest the ability to fabricate a plurality of devices with different functions within a single chip by varying the heights of the cavities. Furthermore, in Lim, there is no description regarding the shape of the cavities in plan view.

The Office cites Fig. 4B and col. 5, lines 1-3 and 9-12, of Lim as disclosing cavities (16) defined by different heights having an opening area with a circular, elliptical, triangular rectangular or other polygonal shape in plan view. However, the sections of Lim cited by the Office do not contain such a description. Lim discloses only that air gaps (16) are formed between the second insulating layer (210) and the first substrate (10B). There is no disclosure or suggestion in Lim that such gaps have varying heights or have the shapes in plan view as recited in claim 16 of the present application.

For these reasons, Lim does not properly support anticipation of claim 16 within the meaning of 35 U.S.C. § 102.

Regarding claim 18 of the present application, the method of Lim fails to include steps which will provide a semiconductor having recessed portions with different depths having an opening area with a circular, elliptical, triangular rectangular or other polygonal shape in plan view as required in claim 18. The Office identifies gaps (16) of Lim as meeting such limitations. However, as explained above, the gaps of Lim do not meet such requirements. Therefore, Lim is also insufficient to the method of claim 18 of the present application within the meaning of 35 U.S.C. § 102.

Rejected claims 21 and 22 depend on claim 18. Therefore, the insufficiency of Lim to support a case of anticipation of claim 18, applies also to the 35 U.S.C. § 102 rejection of claims 21 and 22.

Removal of the 35 U.S.C. 102(e) rejections of claims 16, 18, 21 and 22 is in order and is respectfully solicited.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim.

The propriety of this rejection depends on the propriety of the 35 U.S.C. 102(e) rejection of claim 18, upon which claim 20 depends. Since claim 18 has been shown to be patentable under 35 U.S.C. 102(e) over the disclosure of Lim, claim 20 is *prima facie* patentable.

Applicants also note that when bonding between wafers is carried out in a vacuum atmosphere or a low pressure atmosphere, bonding can be accomplished without regions where there is insufficient bonding (see the paragraph beginning on page 19, line 3, of the specification of the present application). As a result, cavities with higher dimensional precision than the SOI wafers manufactured by the manufacturing method of Lim may be fabricated within a device. Such results cannot be reasonably expected from the disclosure of Lim.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lim in view of Hsu (U.S. Patent No. 6,114,197) (hereinafter: "Hsu").

The propriety of this rejection depends on the propriety of the 35 U.S.C. 102(e) rejection of claim 16, upon which claim 17 depends. Since claim 16 has been shown to be patentable under 35 U.S.C. 102(e) over the disclosure of Lim, claim 17 is *prima facie* patentable.

Applicants also submit that claim 17 is unobvious over the combination of Lim and Hsu proposed by the Office. Hsu discloses a silicon layer 16 and a silicon layer 28 that vary in thickness (Fig. 2 - Fig. 4), but this is nothing more than a disclosure of the formation of silicon layers with varying thicknesses during an intermediate stage in the device formatting process. In the end, all element regions are formed at the same height through the process of fabricating a variety of active regions in these silicon layers by the formation of gate oxidation films and ion implantation. Furthermore, Hsu does not disclose cavities in the device.

A person of ordinary skill in the art would also not be motivated to combine Hsu, which corresponds to an intermediate

stage of device fabrication, and Lim, which discloses a device itself.

Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu in view of Lim.

Hsu discloses silicon layers 28 and 16 with different thicknesses, and a CMOS elemental device is formed on the thin silicon layer 28 (region 18) (see Figs. 2 - 4). However, in Hsu, an ESD diode and an ESD MOS transistor are formed on the silicon layer 16 (regions 20 and 22). Here, the ESD diode and ESD MOS transistor are formed adjacent to the CMOS elemental device for the purpose of preventing damage to the CMOS elemental device by electrostatic discharge (ESD). In other words, Hsu disposes an element for preventing damage to the CMOS element in addition to the CMOS element on a single chip.

In the present invention as recited in claim 23, a functional block using CMOS logic is formed in the thin portion of the active layer and a memory functional block or analog functional block is formed in the thick portion. In other words, a semiconductor device that mixes devices with a plurality of different functions on a single chip may be manufactured easily with the present invention.

Lim discloses cavities within a semiconductor device. However, the cavities in Lim are all of the same height, and in addition, there is no description in Lim regarding the shape of the cavities in a plan view. Thus, the proposed combination of Lim with Hsu, even if proper, would not have provided the semiconductor device of claim 23. For the foregoing reasons, claim 23 of the present invention is not *prima facie* obvious within the meaning of 35 U.S.C. § 103(a) from the combination of Hsu and Lim.

Claims 24-26 depend, directly or indirectly, on claim 23. Therefore, the insufficiencies of the combination of Hsu and Lim to support a *prima facie* case of obviousness of claim 23, apply to claims 24-26.

Removal of the 35 U.S.C. 103(a) rejection of claims 24-26 is also believed to be in order and is respectfully requested.

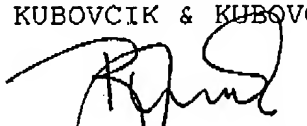
The foregoing is believed to be a complete and proper response to the Office Action dated August 1, 2006, and is believed to place this application in condition for allowance. If, however, minor issues remain that can be resolved by means of a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number indicated below.

In the event that this paper is not considered to be timely filed, applicants hereby petition for an appropriate extension of

time. The fee for any such extension may be charged to our Deposit Account No. 111833.

In the event any additional fees are required, please also charge our Deposit Account No. 111833.

Respectfully submitted,
KUBOVCIK & KUBOVCIK



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